REMARKS

Claim status

Claims 1-32 were pending in the case at the time of the Office Action. Claims 10, and 27-31 are cancelled by this amendment. Claims 1, 2, 4, 5, 6, 8, 9, 11-13, 16-18, 20-26, and 32 are currently amended in the application. Claims 33-58 are newly added by this amendment. Claims 1-9, 11-26, and 32-58 are currently pending in the application.

Drawing rejections

In the current Office action, the Examiner has objected to the drawings by stating that Fig. 1a and Fig. 1c should be designated by a legend such as –Prior Art—because only that which is old is illustrated.

Applicants respectfully traverse the foregoing objection in view of the above amended drawings and for reasons set forth hereafter.

The attached sheet of drawings includes changes to Figs. 1a-1c. This sheet includes Figs. 1a-1c which replaces the original sheet including Figs. 1a-1c. The Examiner's assertion that Fig. 1a and Fig. 1c are admitted prior art is not correct. Fig. 1c was not previously identified as prior art. Fig. 1c is not admitted prior art. Only Fig. 1a is admitted prior art. The figures have been amended to clarify any confusion with respect to admitted prior art by clearly identifying only Fig. 1a as admitted prior art. This amendment is in no way an admission that Fig. 1c is or ever was intended to be identified as admitted prior art. No new matter has been added. Applicants respectfully request that the amended Figures be entered and that the objection be withdrawn.

Specification rejections

The Examiner is requiring, on page 1 of the specification, that "**Summary of the Invention**" be amended to "**Background of the Invention**", as the summary starts on page 3.

In the specification, the heading "**Summary of the Invention**" on page 1 has been amended herein to "**Background of the Invention**" as required by the Examiner. Applicants respectfully request that the amendment be entered as required by the Examiner.

Section 112 second paragraph rejections

In the current Office action, claims 5-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner acknowledges that claims 5-32 would be allowable if rewritten or amended to overcome this rejection(s) under 35 U.S.C. 112, second paragraph.

Applicants respectfully traverse the foregoing rejections in view of the above pending claims and for reasons set forth hereafter.

Claims 5, 6, 8, 9, 11-13, 16-18, 20-26, and 32 have been amended herein to address the Examiner's rejections based on 35 U.S.C. 112, second paragraph. Also, claims 10 and 27-31 are herein cancelled. In view of at least the foregoing, it is respectfully requested that claims 5-9, 11-26, and 32 now define allowable subject matter. Applicants respectfully request that the rejection be removed.

Section 102 and Section 103 rejections

In the current Office action, claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over applicant's admitted prior art.

Applicants respectfully traverse the foregoing rejections in view of the above pending claims and for reasons set forth hereafter.

Independent claim 1 recites a layer structure for Si-based bipolar transistors, comprising a semiconductor layer and an emitter layer formed over the semiconductor layer, wherein thin oxide and/or nitride layers are formed locally between the semiconductor layer and the emitter layer, characterized in that the emitter layer adjoining the semiconductor layer has a mono-crystalline region and, separated from the semiconductor layer by the monocrystalline region, a polycrystalline or amorphous region.

According to page 4, paragraph [0010] of the specification, "the partially monocrystalline emitter layer is locally underlaid with thin oxide and/or nitride layers". Therefore, there is not a contiguous oxide and/or nitride layer between the semiconductor layer

and the emitter layer. Instead, the thin oxide and/or nitride layers are formed locally between the semiconductor layer and the emitter layer. The amendment to claim 1 clearly reflects this fact.

Also, as corrected in the amendments to the drawings, Fig. 1c of the current application is not admitted prior art. Only Fig. 1a is admitted prior art. Fig. 1a does not teach or suggest thin oxide and/or nitride layers formed locally between the semiconductor layer and the emitter layer. According to claim 1, the emitter layer adjoining the semiconductor layer has a monocrystalline region followed by a polycrystalline or amorphous region. There is no monocrystalline region in the emitter layer of Fig. 1a. Paragraph [0015] on page 6 of the specification clearly states, "...and a polycrystalline silicon layer for forming the emitter 5. The current invention provides a monocrystalline section of the emitter layer at the interface between the semiconductor layer 4 and the polycrystalline section 5 of the emitter layer, as can be clearly seen in Fig. 1b. Paragraph [0016] of the specification states with respect to Fig. 1b, "... and in which after initially epitaxial monocrystalline growth of the Si emitter layer 5 ...". Again, Fig. 1a does not teach or suggest a monocrystalline emitter layer.

Also, in the current Office action, claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over U.S. 5,374,481 to Jeng.

Applicants respectfully traverse the foregoing rejections in view of the above pending claims and for reasons set forth hereafter.

Independent claim 1 recites a layer structure for Si-based bipolar transistors, comprising a semiconductor layer and an emitter layer formed over the semiconductor layer, wherein thin oxide and/or nitride layers are formed locally between the semiconductor layer and the emitter layer, characterized in that the emitter layer adjoining the semiconductor layer has a mono-crystalline region and, separated from the semiconductor layer by the monocrystalline region, a polycrystalline or amorphous region.

According to page 4, paragraph [0010] of the specification, "the partially monocrystalline emitter layer is locally underlaid with thin oxide and/or nitride layers". Therefore, there is not a contiguous oxide and/or nitride layer between the semiconductor layer

and the emitter layer. Instead, the thin oxide and/or nitride layers are formed locally between the semiconductor layer and the emitter layer. The amendment to claim 1 clearly reflects this fact.

U.S. 5,374,481 to Jeng does not teach or suggest that thin oxide and/or nitride layers are formed locally between a semiconductor layer and an emitter layer. Instead, U.S. 5,374,481 to Jeng describes a thin interfacial layer deposited between the emitter and the emitter contact (see abstract of U.S. 5,374,481 to Jeng). According to column 2, lines 48-68 of U.S. 5,374,481 to Jeng, the thin interfacial layer is made of material having a wide band gap, such as silicon oxide SiO_x.

There are at least two differences between the layer structure of the present invention of claim 1 and that of U.S. 5,374,481 to Jeng. First, the layer structure of the present invention does not form a contiguous interfacial layer. The oxide and/or nitride layers are only formed locally. There is a clear difference between a contiguous layer and the local formation of an oxide or nitride. Second, the interface under consideration by U.S. 5,374,481 to Jeng is the interface between the emitter and the emitter contact above the emitter layer. In contrast, the interface under consideration in the layer structure of the present invention is the interface between the emitter layer and the semiconductor layer formed below the emitter layer.

Furthermore, U.S. 5,374,481 to Jeng does not teach or suggest providing a monocrystalline section of an emitter layer at a lower interface towards a semiconductor layer. Instead, U.S. 5,374,481 to Jeng is concerned with the opposite interface, namely, between the emitter layer and the emitter contact, and provides a thin interfacial layer between the emitter layer and the emitter contact, which has a wide band gap. This wide band gap film has an electrical function (i.e., it acts as a barrier to reduce hole injection from the base to the emitter contact). U.S. 5,374,481 to Jeng does not teach or suggest providing such an interfacial layer at the interface between the emitter layer and the semiconductor layer underneath. U.S. 5,374,481 to Jeng does not teach or suggest forming an oxide or nitride layer only locally. This would, according to U.S. 5,374,481 to Jeng, make no sense because such a non-contiguous structure would not be able to act as a barrier for holes.

In view of at least the foregoing, it is respectfully submitted that independent claim 1 defines allowable subject matter. Since claims 2-4 depend either directly or indirectly from

claim 1, it is respectfully submitted that dependent claims 2-4 define allowable subject matter as well.

The embodiment of Fig. 1c of the specification corresponds to pending independent claims 33 and 37 in that there is no polycrystalline emitter section, but monocrystalline growth is continued throughout the emitter layer. Support for these claims is found in at least Fig. 1c and paragraphs [0012] and [0017] of the specification.

In view of at least the foregoing, it is also respectfully submitted that new independent claims 33 and 37 define allowable subject matter. Since claims 34-36 and claims 38-58 depend directly or indirectly from claims 33 or 37, it is respectfully submitted that claims 34-36 and 38-58 define allowable subject matter as well.

Accordingly, the applicant respectfully requests reconsideration of the rejections and objections based on at least the foregoing. After such reconsideration, it is urged that allowance of all pending claims will be in order.

Respectfully submitted,

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